Amendments to the Claims:

This listing of claims will replace all prior versions, and lists, of claims in the application:

1-14 (Canceled).

15. (Currently amended) A multiple gate transistor structure comprising:

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed over said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate and at least a second portion of said spacer positioned over said conductive portion of said spacer, wherein said second portion of said spacer is nonconductive;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer wherein said first and second gates cooperate to operate a single transistor.

16. (Previously Presented) A multiple gate transistor as claimed in claim 15 wherein said spacer is formed on a first side of said gate structure to form a second gate and a second side of said gate structure to form a third gate, said second contact being to said conductive portion of said spacer defining said second gate and said multiple gate transistor further comprising a third contact to said conductive portion of said spacer defining said third gate.

17. (Currently amended) A two gate transistor structure comprising:

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary

oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a second portion of said spacer positioned over said first portion of said spacer, wherein said second portion of said spacer is nonconductive;

a first contact to said gate structure; and

a second contact to said conductive portion of said first portion of said spacer wherein said first and second gates cooperate to operate a single transistor.

18. (Currently amended) A three gate transistor structure comprising:

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed over said gate structure;

a first portion of a spacer formed on a first side of said gate structure on said secondary oxide layer, at least a portion of said first portion of said spacer adjacent to said secondary oxide layer being conductive and defining a second gate;

a second portion of said spacer formed on a second side of said gate structure on said secondary oxide layer, at least a portion of said second portion of said spacer adjacent to said secondary oxide layer being conductive and defining a third gate;

a third portion of said spacer positioned over said conductive portion of said first and second portions of said spacer, wherein said third portion of said spacer is nonconductive;

a first contact to said gate structure;

a second contact to said conductive portion of said first portion of said spacer; and

a third contact to said conductive portion of said second portion of said spacer wherein said first, second, and third gates cooperate to operate a single transistor.

19. (Currently amended) An integrated circuit structure comprising:

a first plurality of conventional transistors; and

a second plurality of transistors each comprising:

a first oxide layer formed on a semiconductor structure;

a gate structure formed on said first oxide layer defining a first gate:

a secondary oxide layer formed on said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate and at least a second portion of said spacer positioned over said conductive portion of said spacer, wherein said second portion of said spacer is nonconductive;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer wherein said first and second gates cooperate to operate a single transistor and said first plurality of conventional transistors and said second plurality of transistors are interconnected to form said integrated circuit structure.

20-22 (Canceled).

23. (Currently Amended) A transistor structure comprising:

a first oxide layer formed on said semiconductor substrate;

a gate structure formed on said first oxide layer defining a first actual gate and a first pseudo gate;

a secondary oxide layer formed over said actual and pseudo gates;

a spacer formed on at least one side of said actual gate and on said pseudo gate on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate and at least a second portion of said spacer positioned over said conductive portion of said spacer, wherein said second portion of said spacer is nonconductive;